



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/900,946	07/10/2001	Fumio Hirahara	211134US2S	7965

22850 7590 04/24/2002

OBLON SPIVAK MCCLELLAND MAIER & NEUSTADT PC  
FOURTH FLOOR  
1755 JEFFERSON DAVIS HIGHWAY  
ARLINGTON, VA 22202

EXAMINER

MITCHELL, JAMES M

ART UNIT	PAPER NUMBER
----------	--------------

2827

DATE MAILED: 04/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/900,946

Applicant(s)

HIRAHARA ET AL.

Examiner

James Mitchell

Art Unit

2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 10 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

1. This office action is in response to the supplemental papers filed July 10, 2001.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2, 3, 5 and 7-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 2 recites the limitation "the other end ". There is insufficient antecedent basis for this limitation in the claim.

5. In regards to claim 5, it is ambiguous as to whether a current in the opposite direction is equivalent to a reverse bias? If not, what characteristics distinguish a current in an opposite direction? Does the device's on and off state affect the opposite direction? Is the current that flows in the opposite direction exhibited by at least two terminals, such that the two terminals currents are in the same direction or are the currents of the two terminals in opposite direction?

6. In regards to claim 7, it is unclear to how the word control further limits the scope of the word electrode.

7. Claims 9 and 10 recite the limitation "the power terminal positioned on one end of said power terminal or/and on the other end." There is insufficient antecedent basis for these limitations in the claims. Furthermore, claim 4 from which claim 10 depends

Art Unit: 2827

indicates that the power terminals are connected and pressure welded to the semiconductor chip, not another power terminal as indicated in claim 10.

8. As such, claims 5, 9 and 10 have not been rejected over the prior art because, in light of the 35 U.S.C. 112 rejections supra, there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of the claims; hence, it would not be proper to reject the claims on the basis of prior art. As stated in *In re Steele*, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims. See also MPEP 2173.06.

***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

((b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuda (EP 0588094).

11. Matsuda discloses (Fig 1; Column 6, Lines 2-6) a plurality of semiconductor chips comprising a transistor (29) that inherently comprises an insulation layer and a diode (31), at least three power terminals (3,5,7) superimposed on each other, and at least one semiconductor chip sandwiched between a predetermined said two terminals in a device for large power (Column 1, Lines 5-7), wherein a portion of a terminal (defined by

the top portion of the terminals 3 & 5) on one end among superposed power terminals of a power terminal and a power terminal on the other end among said superposed power terminals are led out in the same direction (3,5), wherein the middle terminal (5, via the top portion) is led out in a direction opposite to a power terminal (7), with at least a first and second face of said semiconductor chip connected to a first and second power terminal through soldering (Column 6, Lines 3-6; via both the chip and terminals being attached to substrate, 15), and a control electrode (17) and electrode pad (inherent pad formed on chip) connected by wirebonding (Column 6, Lines 32-35).

#### ***Allowable Subject Matter***

13. Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nakatsuka (U.S 6,208,521), Hiroyuki (JP 07-202072).

The prior art discloses in Nakatsuka and Hiroyuki the use of a chip sandwiched between superimposed terminals.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

Art Unit: 2827

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3230 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

*JMM*  
Jmm

April 19, 2002

*David E. Graybill*  
DAVID E. GRAYBILL  
PRIMARY EXAMINER